What Is Claimed Is:

1. A charged-device model (CDM) electrostatic discharge (ESD) protection circuit for an integrated circuit (IC), the ESD protection circuit comprising:

an ESD clamp device, coupled to a pad and a substrate having a first conductivity type, the ESD clamp device being closed under normal power operation; and

a functional component, formed on the substrate and coupled to the pad, the functional component having a first well of the first conductivity type and an isolating region of a second conductivity type, the second conductivity type being the reversed polarity of the first conductivity type, and the isolating region isolating the first well from the substrate; the functional component transmitting signals between the IC and an external linkage under normal power operation.

2. The CDM ESD protection circuit in claim 1, wherein when the isolating region comprises a second well surrounding the first well and a deep well under the first well.

3. The CDM ESD protection circuit in claim 1, wherein the isolating region is coupled to a first power supply and the first well is coupled to a second power supply.

4. The CDM ESD protection circuit in claim 1, wherein the functional component comprises a metal-oxide semiconductor (MOS) having the second conductivity type in the first well.

5. The CDM ESD protection circuit in claim 1, wherein the ESD clamp device comprises an MOS diode having two ends respectively coupled to the pad and the substrate.

6. The CDM ESD protection circuit in claim 1, wherein the ESD clamp device is a two-stage ESD protection circuit, having a primary ESD protection circuit coupled between the pad and the substrate, a secondary ESD protection circuit coupled between the functional component and the substrate, and a resistor coupled between the functional component and the pad.

7. The CDM ESD protection circuit in claim 1, wherein the first conductivity type is an N type, and the second conductivity type is p type.

8. The CDM ESD protection circuit in claim 1, wherein the first conductivity type is a p type, and the second conductivity type is N type.

9. A charged-device model (CDM) electrostatic discharge (ESD) protection circuit for an input port of an integrated circuit (IC), the ESD protection circuit comprising:

an ESD clamp device, coupled to a pad and a substrate having a first conductivity type, under normal power operation, the ESD clamp device being closed; and

an MOS component having a second conductivity type, formed in a first well on the substrate and coupled to the pad; an isolating region having the second conductivity type being formed between the first well and the substrate to separate the first well and the substrate, the second conductivity type being

the reversed polarity of the first conductive type, and under normal power operation, the MOS component transmitting signals from the pad into the IC.

10. The CDM ESD protection circuit in claim 9, wherein a gate of the MOS component is coupled to the pad.

11. The CDM ESD protection circuit in claim 9, wherein the source of the MOS component is coupled to an internal power line.

12. The CDM ESD protection circuit in claim 11, wherein the CDM ESD protection circuit further comprises an ESD protection circuit coupled between the gate of the MOS component and the internal power line.

13. The CDM ESD protection circuit in claim 12, wherein the ESD protection circuit at the input port is an gate-grounded MOS component.

14. The CDM ESD protection circuit in claim 11, wherein the first well is coupled to the internal power line.

15. A charged-device model (CDM) electrostatic discharge (ESD) protection circuit for an output port of an integrated circuit (IC), the ESD protection circuit comprising:

an ESD clamp device, coupled to a pad and a substrate having the first conductivity type, under normal power operation, the ESD clamp device being closed; and

an MOS component having a second conductivity type, formed in a first well on the substrate and coupled to the pad; an

isolating region having the second conductivity type being formed between the first well and the substrate to separate the first well and the substrate, the second conductivity type being the reversed polarity of the first conductive type, and under normal power operation, the MOS component transmitting signals from the IC to the pad.

16. The CDM ESD protection circuit in claim 15, wherein a drain of the MOS component is coupled to the pad, a source of the MOS component and the first well are coupled to an I/O power line.

17. The CDM ESD protection circuit in claim 15, wherein a plurality of diodes are disposed between the I/O power line and an internal power line.

18. A CDM ESD protection circuit, suitable for an I/O port of a high voltage IC, the CDM ESD protection circuit comprises:

an ESD clamp device, coupled between a pad and a p-type substrate, the ESD clamp device being closed under normal power operation; and

a first NMOS (N-type metal-on-semiconductor) component formed on a P-type first isolated well on the substrate, an N-type isolating region being formed to separate the P-type first isolated well and the substrate; the NMOS component having a gate coupled to a high power line, a first source/drain coupled the pad, and a second source/drain coupled to an input buffer; and

an output driver comprising a second and a third NMOS component respectively formed in a P-type second isolated well on the substrate and connected in series; an N-type second

isolating region formed between the P-type second isolated well and the substrate, a gate of the second NMOS component, coupled to the high Power line, a drain of the second NMOS component coupled to the pad, a source of the second NMOS component coupled to a drain of the third NMOS component, a source of the third NMOS component coupled to an I/O low power line, and a gate of the third NMOS component being to a pre-output driver.

19. The CDM ESD protection circuit in claim 18, wherein the first isolated well is coupled to an internal low power line, the second isolated well is coupled to the I/O low power line.

20. The CDM ESD protection circuit in claim 19, wherein a plurality of diodes are disposed between the internal low power line and the I/O low power line.

21. The CDM ESD protection circuit in claim 18, wherein the ESD clamp device comprises a forth NMOS component and a fifth NMOS component, connected in series between the pad and I/O low power line, a gate of the forth NMOS component is coupled to the high power line, and a gate of the fifth NMOS component is coupled to the I/O low power line.

22. The CDM ESD protection circuit in claim 18, wherein an ESD protection resistor is formed between the first NMOS component and the pad.